Hierarchical Fault Tracing VLSI Sequential Circuit by Successive Circuit Extraction from CAD Layout Data

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Abstract: A hierarchical VLSI fault tracing method is proposed which is applicable to the case where only CAD layout data is available in the CAD-linked electron beam test system. The CAD layout data is assumed to be hierarchically structured. The method uses the expansion of a previously proposed integrated algorithm which combines a transistor-level fault tracing algorithm and a successive circuit extraction from a non-hierarchically or a flat structured CAD layout data. The method allows us to trace a fault hierarchically from the top level cell to the lowest primitive cell and from the primitive cell to the transistor-level circuit in a consistent manner independent of circuit functions even when the cell data and the transistor-level circuit data exist in a level as a mixture. An application of the method to a hierarchically structured CMOS model layout with about 600 transistors shows its validity.

Keywords: fault tracing, CAD layout data, successive circuit extraction, sequential circuit, benchmark circuit

1. Introduction

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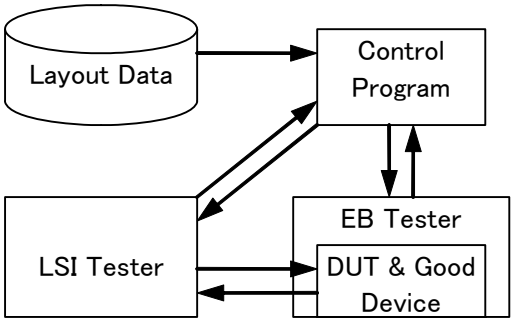

Fig. 1 An example of the figure

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4. Conclusions

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Table 1 An example of the table

Circuit name	# of transis-tors	# of probing points
S27	136	6.6
S208	676	14.9
S298	1006	10.9

Acknowledgements

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References

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